

# **Metrology Challenges for Nanotechnology-A Semiconductor Manufacturer's Perspective**

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## **ABSTRACT**

There are numerous metrology challenges facing semiconductor manufacturing for the 32 nm technology node and beyond in the areas of critical dimension (CD), overlay, films and defect metrology. Many of these challenges are identified in the 2005 *International Technology Roadmap for Semiconductors* (ITRS). The metrology sections of the ITRS call for measurement of 32/22/18 nm generation devices. Each subsequent technology generation requires less process control variation, which results in a continuing need for improved metrology precision. In addition, there is an increasing need to understand individual edge variation and edge placement errors relative to the intended design. This is driving an accelerating need for new methods of measurement, as well as new target structures. This presentation will provide an overview of the metrology challenges for semiconductor manufacturing, taking into account the areas addressed in the 2005 ITRS for the 45 nm technology generation and beyond.